

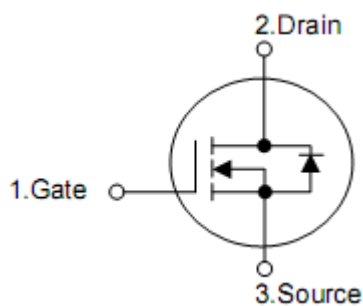
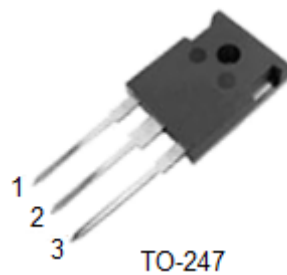
## 1. Product Features

- $R_{DS(ON),typ.}=2.8\Omega@V_{GS}=10V$
- Low Gate Charge Minimize Switching Loss
- Fast Recovery Body Diode

## 2. Applications

- Adaptor
- Charger
- SMPS Standby Power

## 3. Pin configuration



Pin	Function
1	Gate
2	Drain
3	Source

## 4. Ordering Information

Part Number	Package	Brand
KNM48150A	TO-247	KIA

## 5. Absolute maximum ratings

(T<sub>C</sub>= 25°C , unless otherwise specified)

Parameter	Symbol		Unit	
Drain-to-Source Voltage <sup>1)</sup>	V <sub>DSS</sub>	1500	V	
Gate-to-Source Voltage	V <sub>GSS</sub>	±30		
Continuous Drain Current	I <sub>D</sub>	9	A	
Pulsed Drain Current at V <sub>GS</sub> =10V	I <sub>DM</sub>	36		
Single Pulse Avalanche Energy	E <sub>AS</sub>	450	mJ	
Maximum Power Dissipation	P <sub>D</sub>	T <sub>C</sub> =25°C	320	W
		Derate above 25°C	2.56	W/°C
Soldering Temperature Distance of 1.6mm from case for 10 seconds	T <sub>L</sub>	300	°C	
Storage Temperature Range	T <sub>J</sub> &T <sub>STG</sub>	-55 to 150		

Caution: Stresses greater than those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device.

## 6. Thermal characteristics

Parameter	Symbol	Rating	Unit
Thermal Resistance, Junction-to-Case	R <sub>θJC</sub>	0.39	°C/W
Thermal Resistance, Junction-to-Ambient	R <sub>θJA</sub>	55	°C/W

## 7. Electrical characteristics

 (T<sub>J</sub>=25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Drain-source breakdown voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	1500	-	-	V
Drain-source leakage current	I <sub>DSS</sub>	V <sub>DS</sub> =1500V, V <sub>GS</sub> =0V	-	-	1	uA
		V <sub>DS</sub> =1200V, T <sub>C</sub> =125°C	-	-	500	uA
Gate-source forward leakage	I <sub>GSS</sub>	V <sub>GS</sub> =±30V, V <sub>DS</sub> =0V	-	-	±100	nA
Drain-source on-resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =5.4A	-	2.8	4	Ω
Gate threshold voltage	V <sub>GS(TH)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250uA	2.5	-	4.5	V
Gate Resistance	R <sub>g</sub>	f=1 MHz Gate DC Bias=0, Test signal level=20mVopen drain	-	1.17	-	Ω
Input capacitance	C <sub>iss</sub>	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V f=1MHz	-	3385	-	pF
Reverse transfer capacitance	C <sub>rss</sub>		-	54.6	-	pF
Output capacitance	C <sub>oss</sub>		-	176	-	pF
Total gate charge(10V)	Q <sub>g</sub>	V <sub>DD</sub> =750V, I <sub>D</sub> =9A V <sub>GS</sub> =0~10V	-	68	-	nC
Gate-source charge	Q <sub>gs</sub>		-	21	-	nC
Gate-drain charge	Q <sub>gd</sub>		-	25	-	nC
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> =750V, V <sub>GS</sub> =10V, R <sub>G</sub> =25Ω, I <sub>D</sub> =9A	-	65	-	ns
Rise time	t <sub>r</sub>		-	186	-	ns
Turn-off delay time	t <sub>d(off)</sub>		-	82	-	ns
Fall time	t <sub>f</sub>		-	114	-	ns
Continuous Source Current <sup>2)</sup>	I <sub>SD</sub>	Integral PN-diode in MOSFET	-	-	9	A
Pulsed Source Current <sup>2)</sup>	I <sub>SM</sub>		-	-	36	A
Diode forward voltage	V <sub>SD</sub>	I <sub>S</sub> =9A, V <sub>GS</sub> =0V,	-	-	1.3	V
Reverse Recovery Time	t <sub>rr</sub>	V <sub>GS</sub> =0V, I <sub>F</sub> =9A, dI <sub>F</sub> /dt=100A/μs	-	461	-	nS
Reverse Recovery Charge	Q <sub>rr</sub>		-	3.36	-	nC

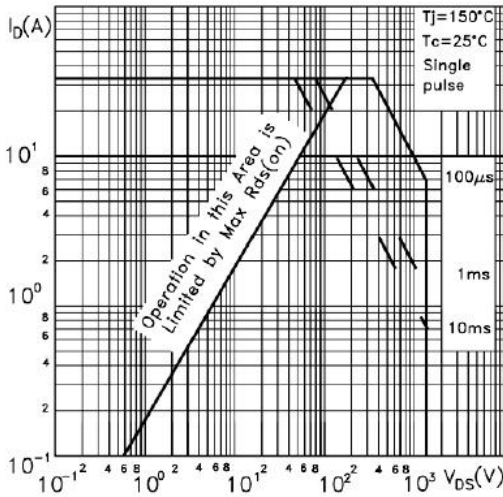
Note:

 1) T<sub>J</sub>=+25°C to +150°C

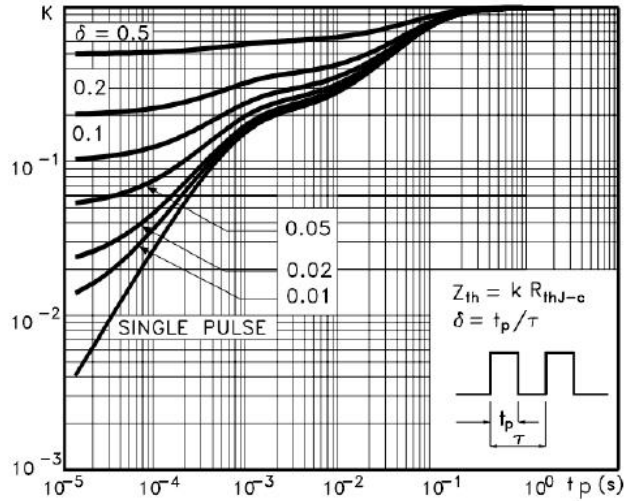
2) Pulse width≤380us; duty cycle≤2%.

**8. Test circuits and waveforms**

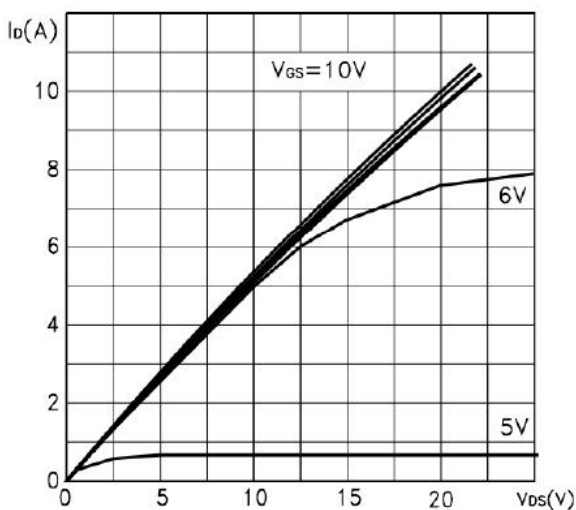
**Figure 1.Safe operating area**



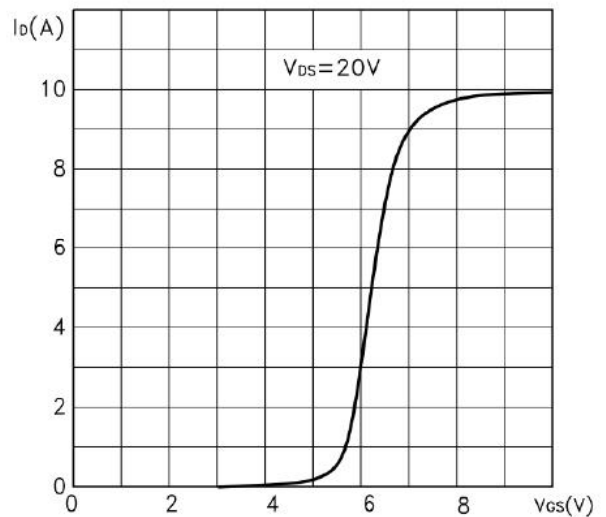
**Figure 2.Thermal impedance**



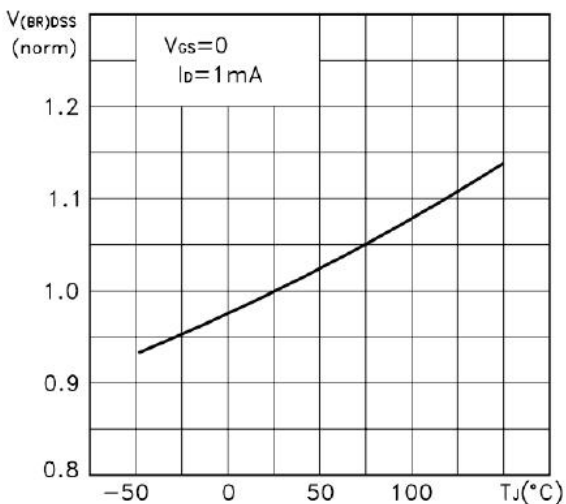
**Figure 3.Output characteristics**



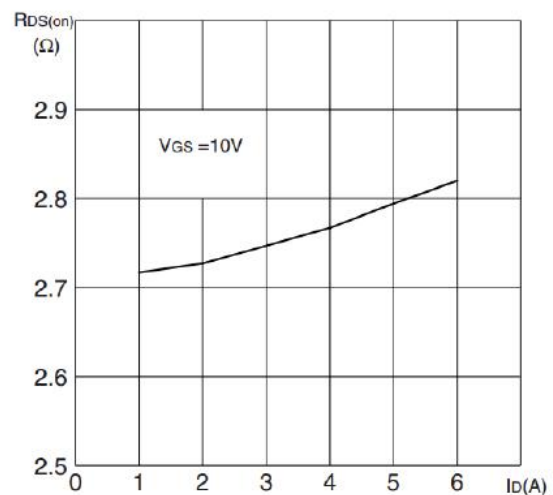
**Figure 4.Transfer characteristics**



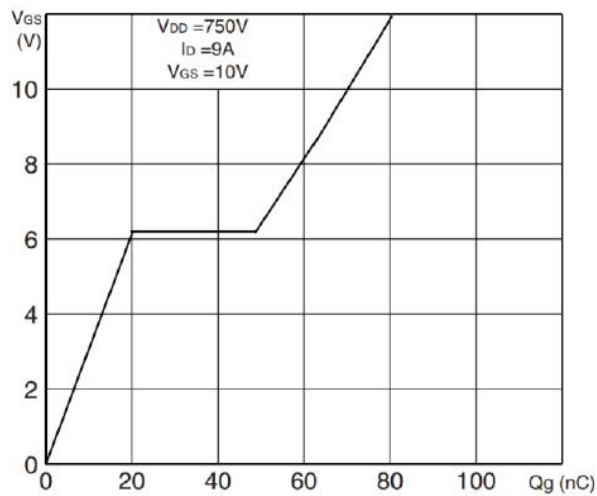
**Figure 5.Normalized  $BV_{DSS}$  vs temperature**



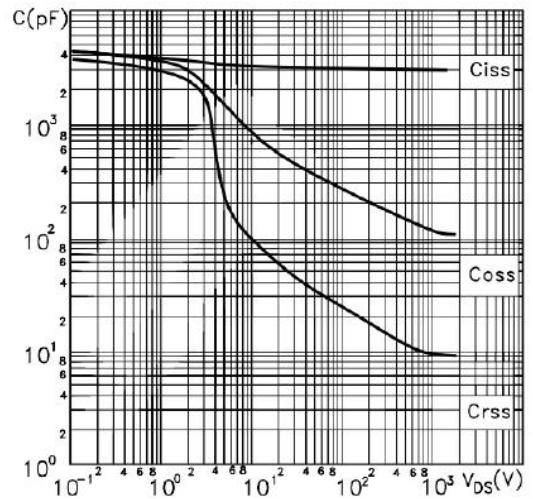
**Figure 6.Static drain-source on resistance**



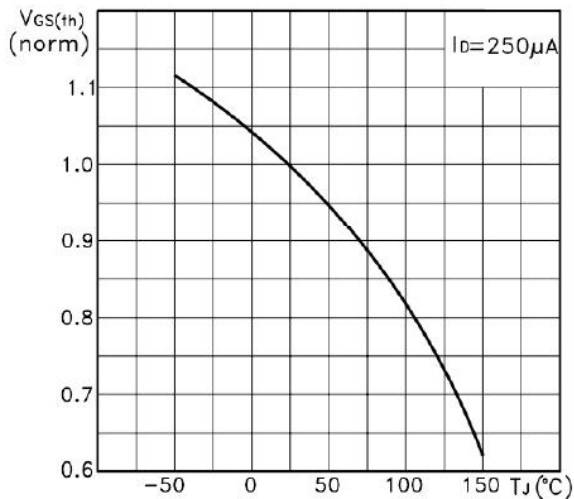
**Figure 7. Gate charge vs gate-source voltage**



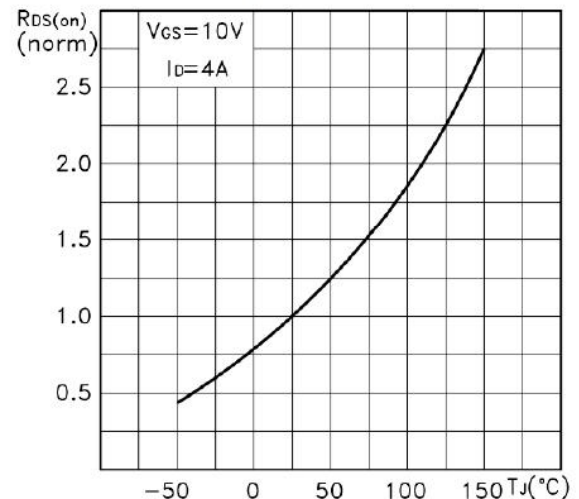
**Figure 8. Capacitance variations**



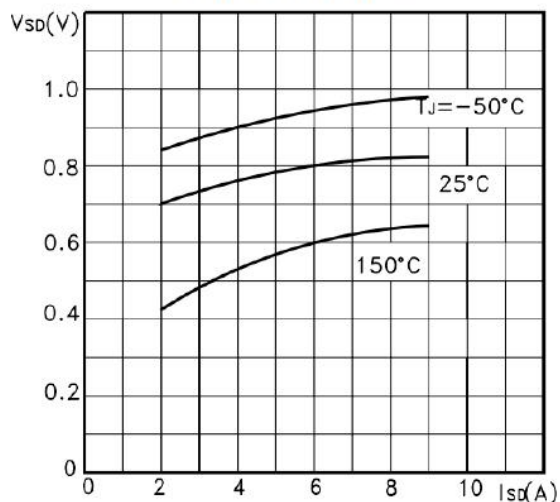
**Figure 9. Normalized gate threshold voltage vs temperature**



**Figure 10. Normalized on resistance vs temperature**



**Figure 11. Source-drain diode forward characteristics**



**9. Test Circuits and Waveform**

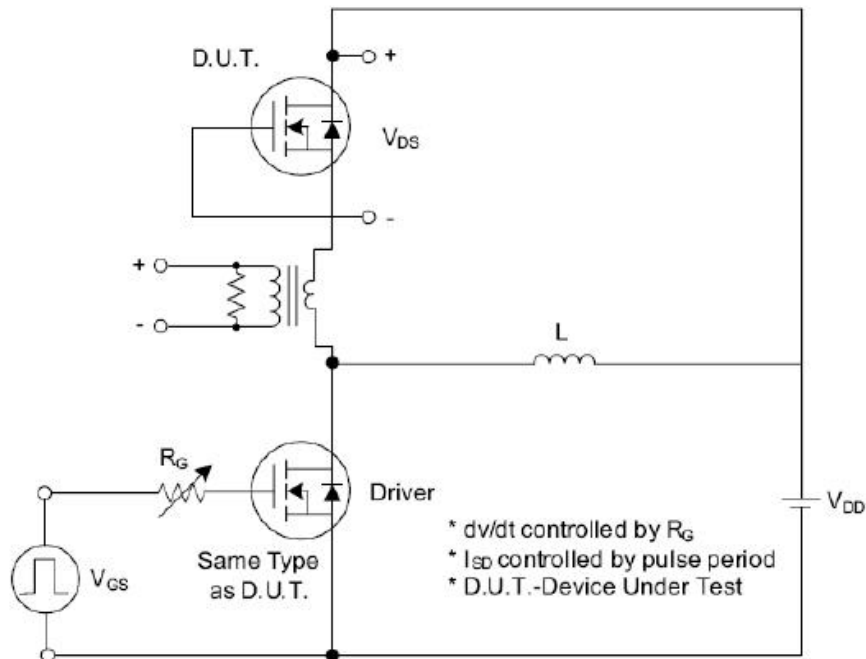


Fig. 1.1 Peak Diode Recovery  $dv/dt$  Test Circuit

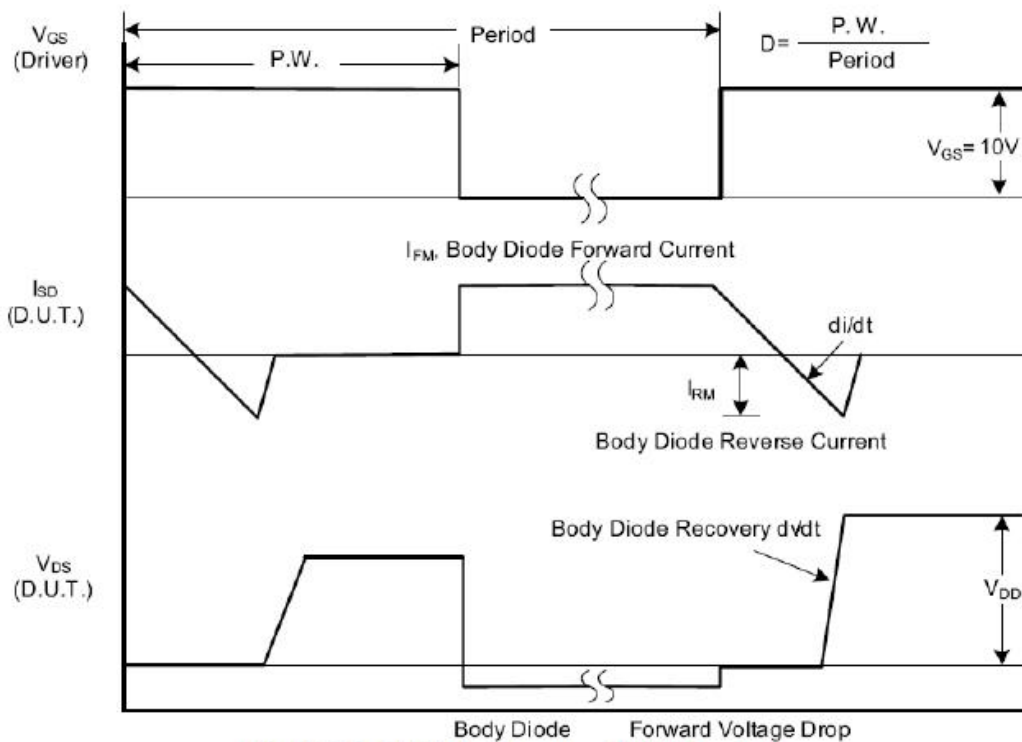


Fig. 1.2 Peak Diode Recovery  $dv/dt$  Waveforms

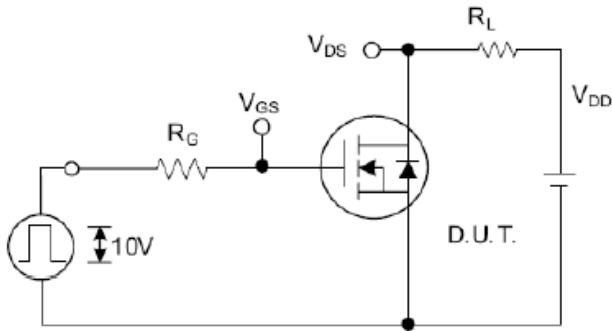


Fig. 2.1 Switching Test Circuit

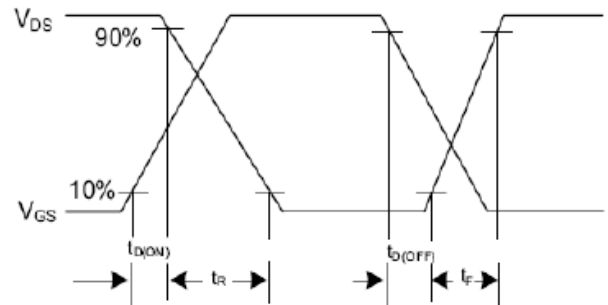


Fig. 2.2 Switching Waveforms

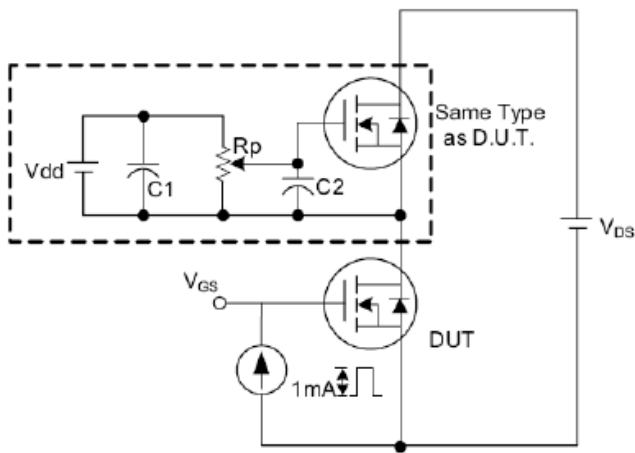


Fig. 3.1 Gate Charge Test Circuit

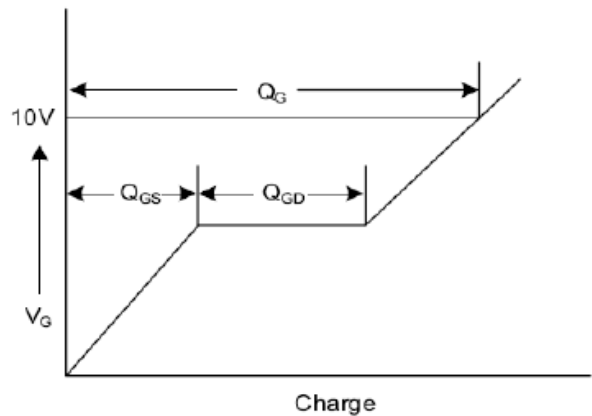


Fig. 3.2 Gate Charge Waveform

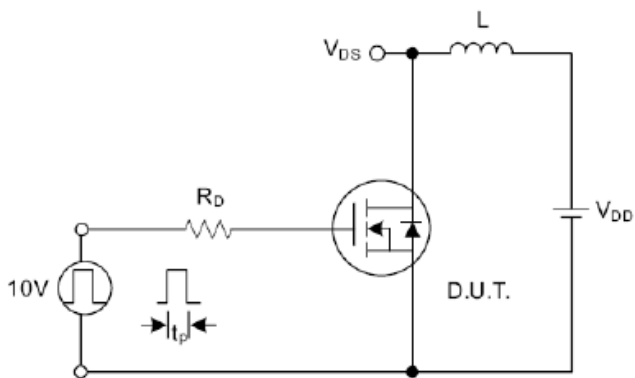


Fig. 4.1 Unclamped Inductive Switching Test Circuit

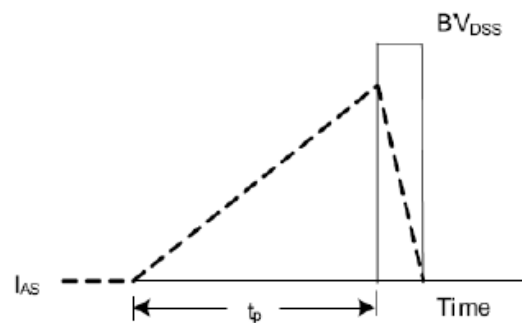


Fig. 4.2 Unclamped Inductive Switching Waveforms